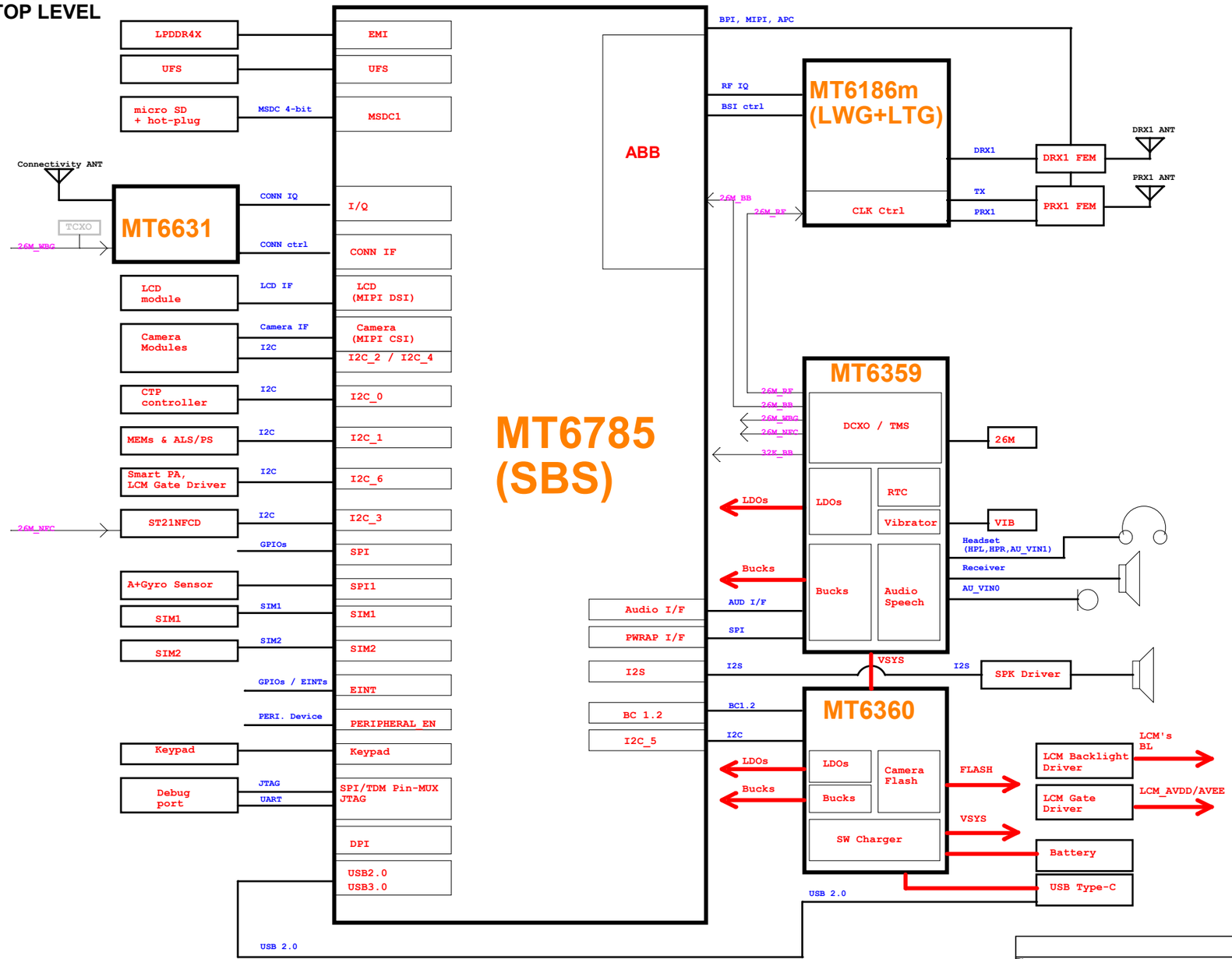
Project : MT6785 LPDDR4X
REF_SCH TOP LEVEL



Title: 01_Block_Diagram

Size: C

MTK Confidential

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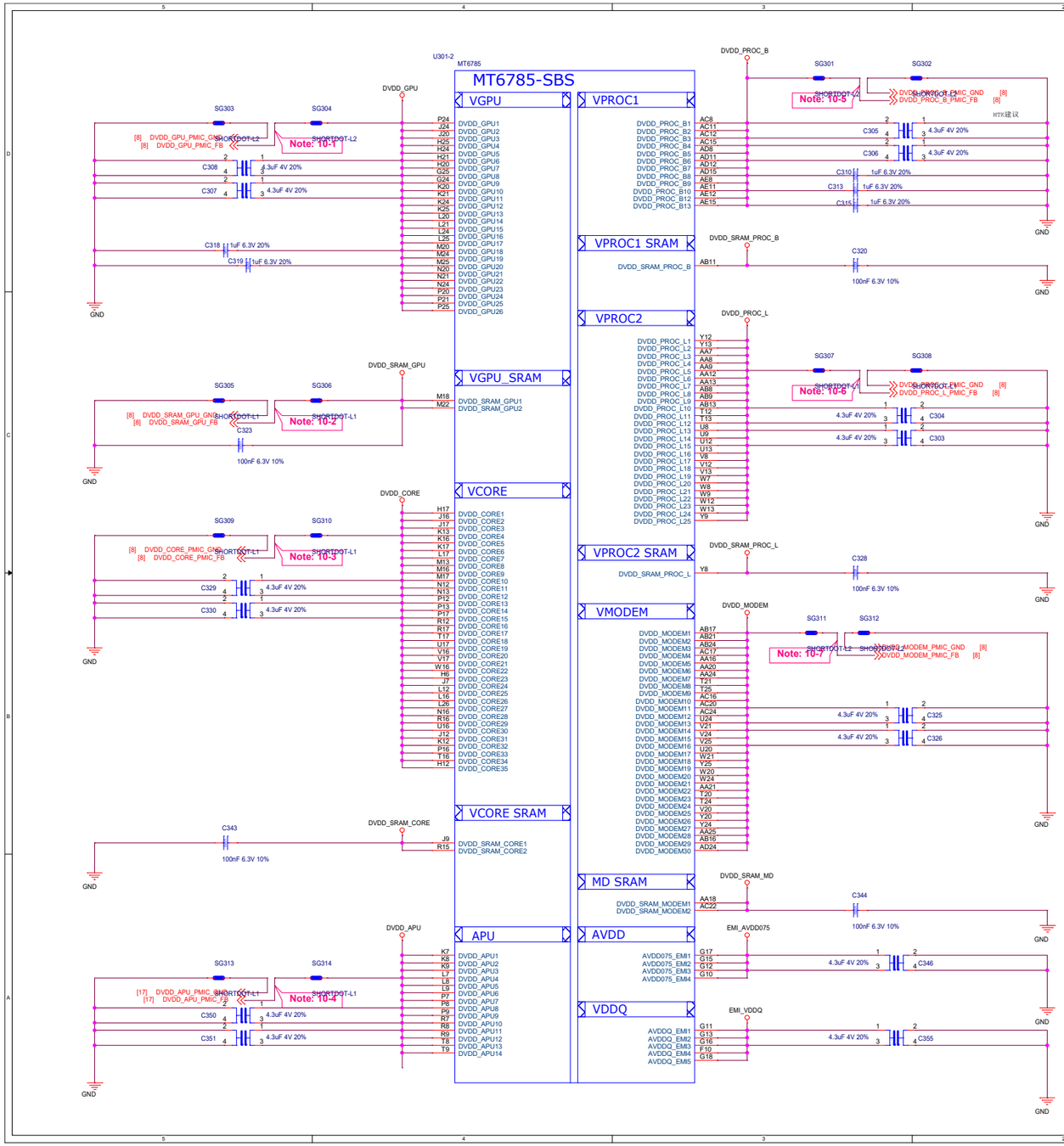

Schematic design notice of "10_BB_POWER_PDN" page.

Note 10-1:	Differential pair of DVDD_GPU remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-2:	Differential pair of DVDD_SRAM_GPU remote sense must be close to 22uF due to SRAM application. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-3:	Differential pair of DVDD_CORE remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-4:	Differential pair of DVDD_APU remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-5:	Differential pair of DVDD_PROC_B remote sense must be close to BB's ball Remote sense trace with GND shielding to PMIC (Differential)
Note 10-6:	Differential pair of DVDD_PROC_L remote sense must be close to BB's ball Remote sense trace with GND shielding to PMIC (Differential)
Note 10-7:	Differential pair of DVDD_MODEM remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)

Title: 03_BB_POWER_PDN

Size: C

MTK Confidential

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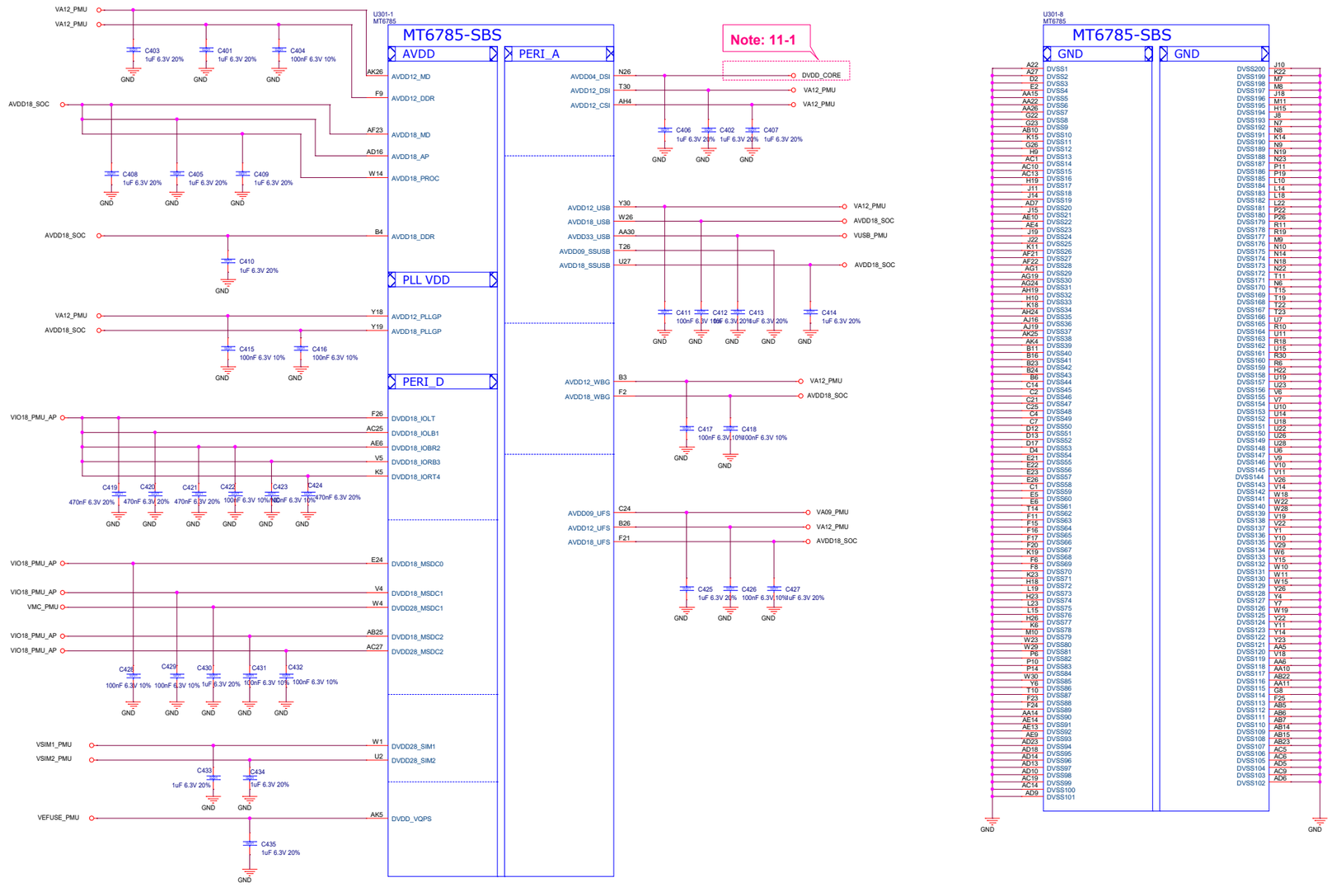

Schematic design notice of "11_BB_POWER_IO" page.

Note 11-1: For D-PHY application, connect MIPI Power domain AVDD04_DSI to DVDD_CORE.
For C-PHY application, connect MIPI Power domain AVDD04_DSI to VA12_PMU.

Title	04_BB_POWER_IO
Size C	MTK Confidential
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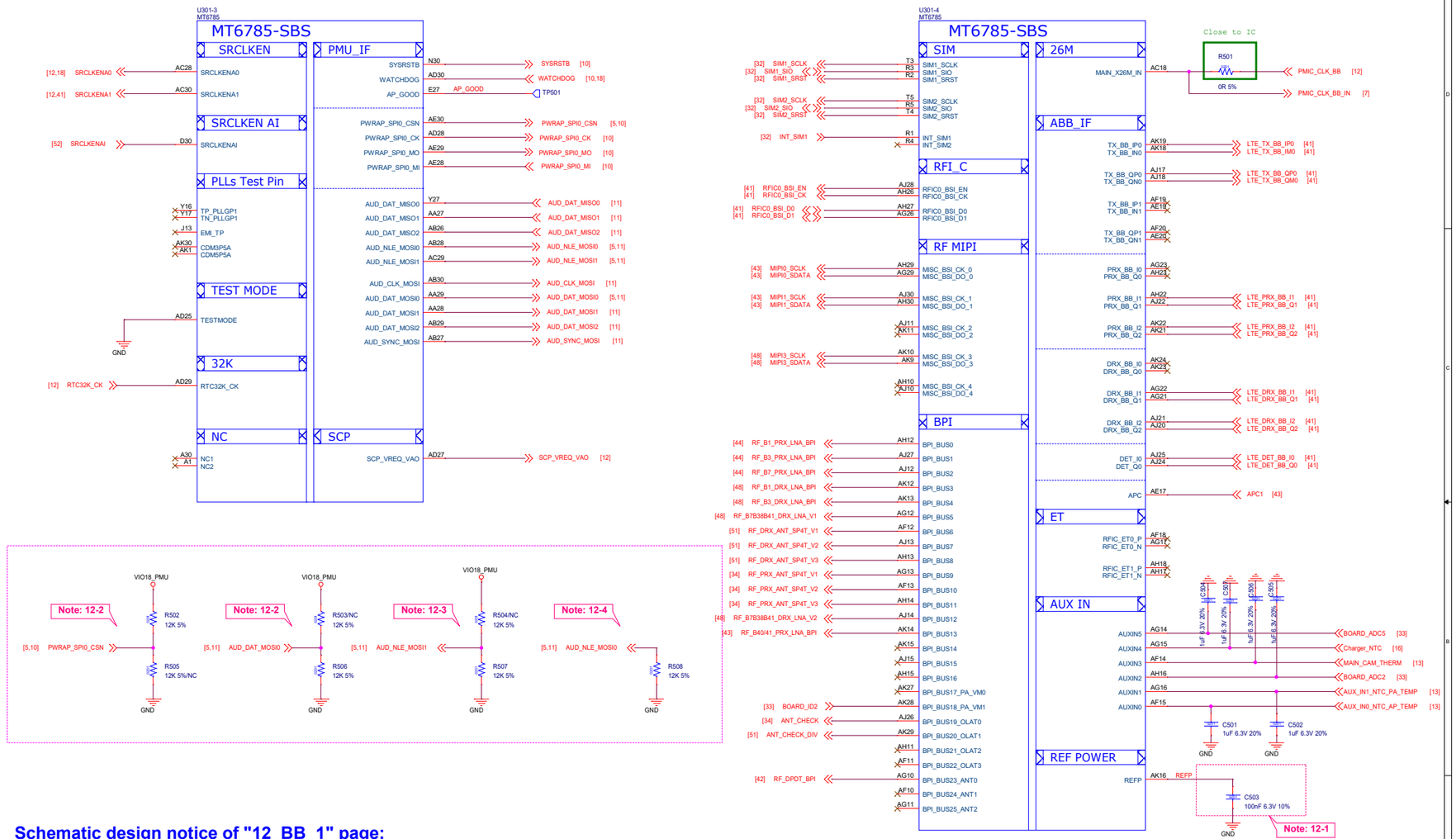

Schematic design notice of "12_BB_1" page:

Note 12-1: The de-coupling cap. for REFP (AK16 ball) have to be placed as close to BB as possible.

Note 12-2: PWRAP_SPI0_CSN and AUD_DAT_MOSI are JTAG feature in bootstrap.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP_JTAG	IO_JTAG
HI	LO	N/A	N/A
HI	HI (by external PU)	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT3	N/A
LO (by external PD)	LO	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT3	TDM_LRCK/TDM_BCK/TDM_MCLK/ TDM_DATA0/TDM_DATA1
LO (by external PD)	HI (by external PU)	MSDC1_CLK/CMD/ DAT0/DAT1/DAT2	N/A

Note 12-3: AUD_NLE_MOSI1 is USB JTAG feature in bootstrap.

AUD_NLE_MOSI1	USB JTAG
LO	USB 2.0
HI (by external PU)	DP/DM output JTAG

Note 12-4: AUD_NLE_MOSI0 is storage booting feature in bootstrap.

AUD_NLE_MOSI0	Storage Booting
LO	UFS only
HI (by external PU)	eMMC only

Title: 05_BB_1

Size: C

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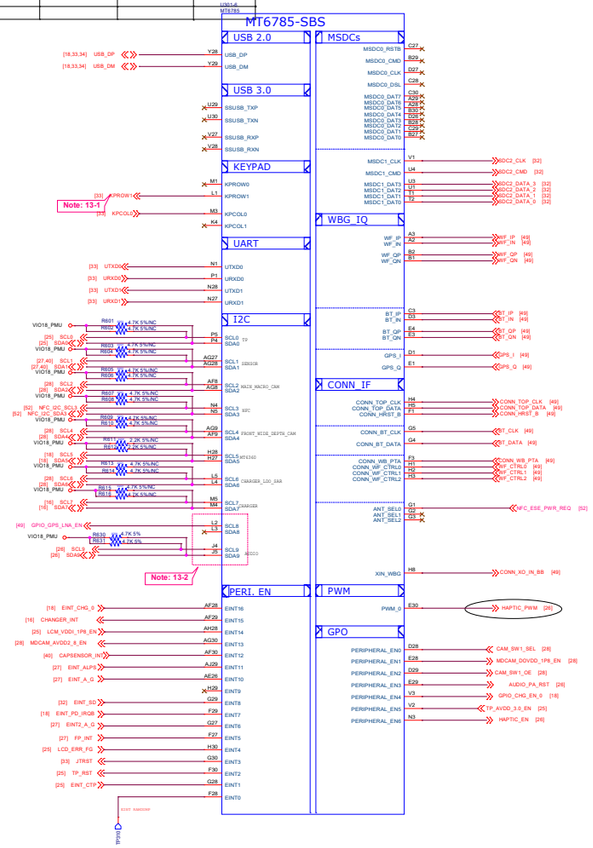
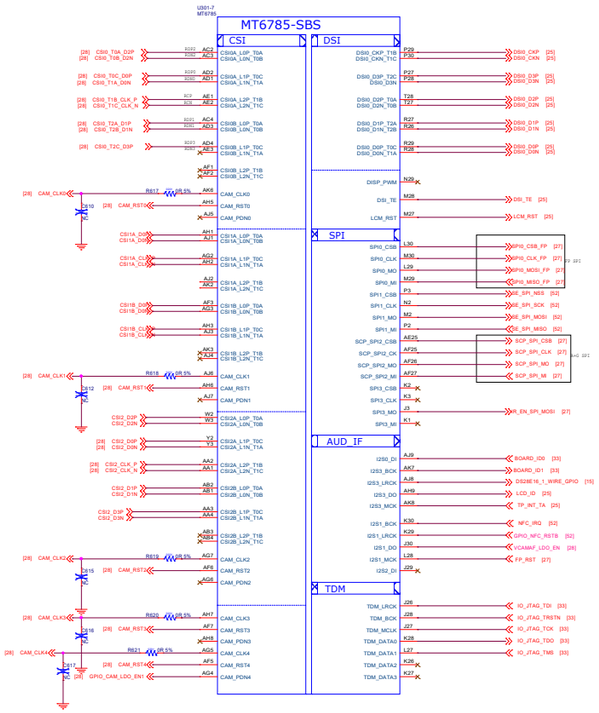
I2C	Device1	Device2	Device3	Device4	Device5	Device6
0	CTP					
1	TSL2540 0x29	BU27030NUC 0x38	AK09918C 0x0C	Sar_SENSOR		
2	Main_CAM	Macro_CAM				
3	NFC ST21					
4	Front_CAM	Depth_CAM				
5	MT6360					
6	ML2866D-10/TR 0x64	Wide_CAM				
7	SC8551					
9	AW87559FCR	AW87389FCR				





Schematic design notice of "06_BB_2" page.

Note 13-1: Reserved for fast META mode detection

Note 13-2: For (I2C-8, I2C-9), must have pull up resistor 4.7K ohm for standard mode and fast mode; 2.2K ohm for fast mode plus and high speed mode.

File: 06_BB_2

Size: D

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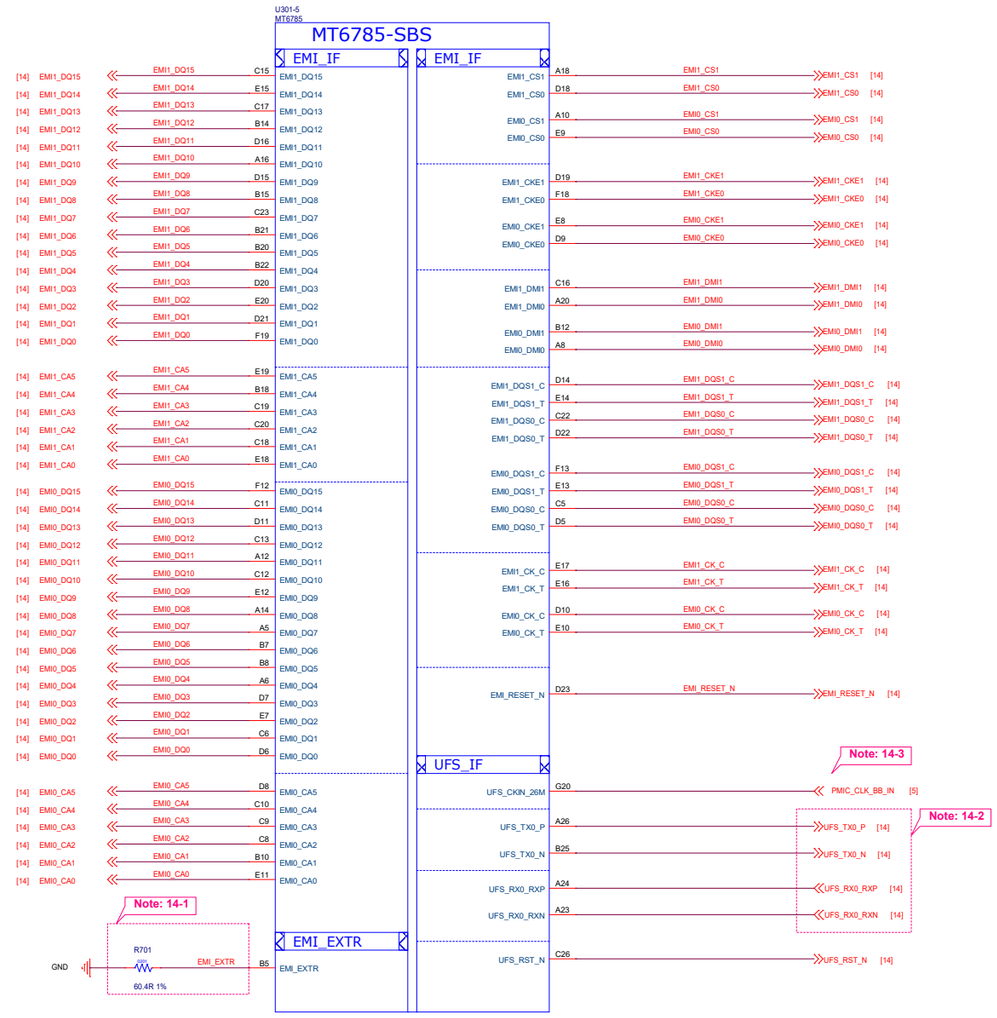

Schematic design notice of "14_BB_3_Interface" page:

Note 14-1:	R4001 please select 60.4 ohm (1%) resistor
Note 14-2:	Make sure TX/RX connection (T to in, R to out and P to t, N to c)
Note 14-3:	UFS IP use 26MHz clock from PMIC XO_SOC (shared with ABB IF) and UFS device from PMIC XO_EXT. All of their layout must be shielded by GND.

Title: 07_BB_3

Size: C

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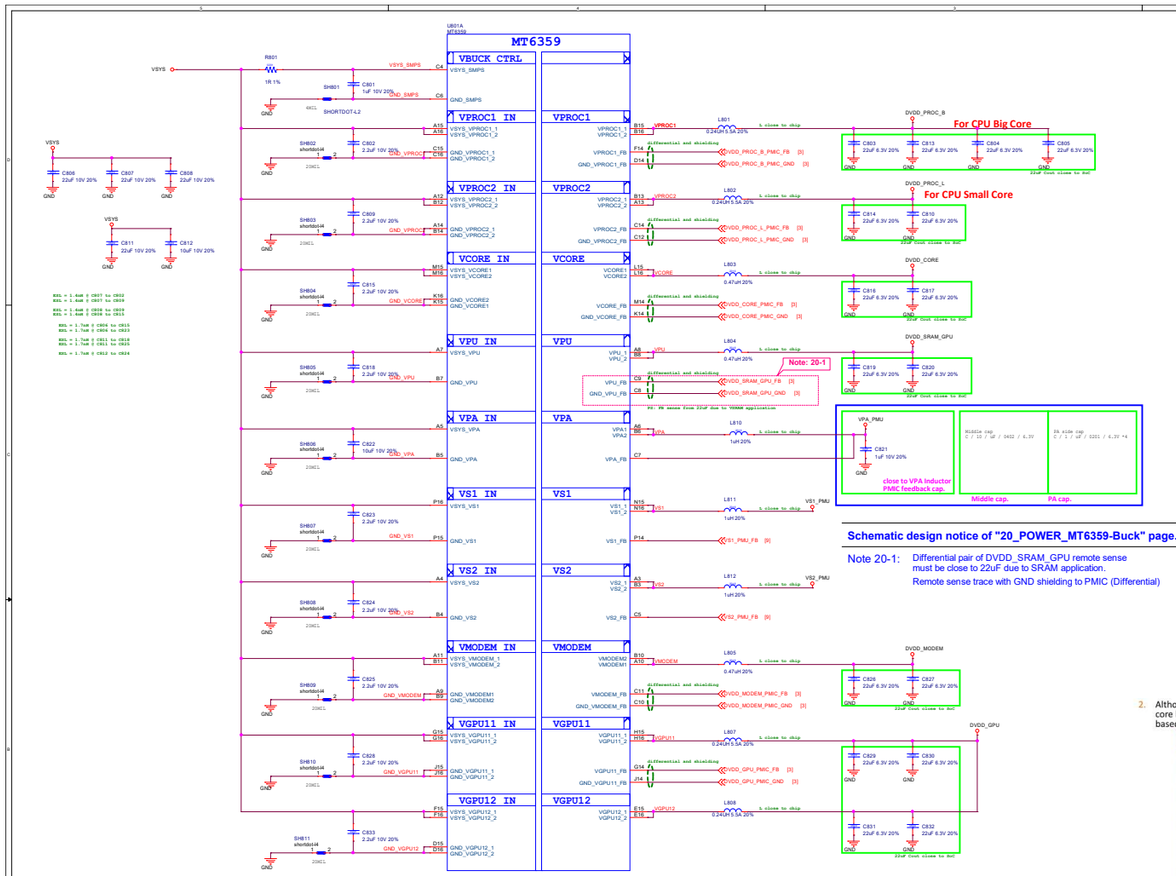

Schematic design notice of "20_POWER_MT6359-Buck" page.

Note 20-1: Differential pair of DVDD_SRAM_GPU remote sense must be close to 22uF due to SRAM application.
Remote sense trace with GND shielding to PMIC (Differential)

2. Although small size and high efficiency are major concerns, the inductor should have low core losses and low DCR (copper wire resistance). Efficiency data in MT6359 datasheet is based on 30mΩ DCR.

BUCK	Inductance (uH)	$I_{SAT,MAX}$ (A)	$I_{TEMP,MAX}$ (A)
VS1	1.0	2.6	2.0
VS2	1.0	2.6	2.0
VPA	1.0	4.0	3.4
VMODEM	0.47	4.8	4.2
VPROC1	0.24	6.3	5.0
VPROC2	0.24	6.1	4.8
VCORE	0.47	5.5	4.8
VGPU11	0.24	6.3	5.0
VGPU12	0.24	6.3	5.0
VPU (SRAM_GPU)	0.47	1.3	0.6

MEDIATEK Note: Depends on inductance saturation. (-30% reduction from Initial L value)

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<Variant Name>
File: 08_POWER_MT6359-Buck
Size: D
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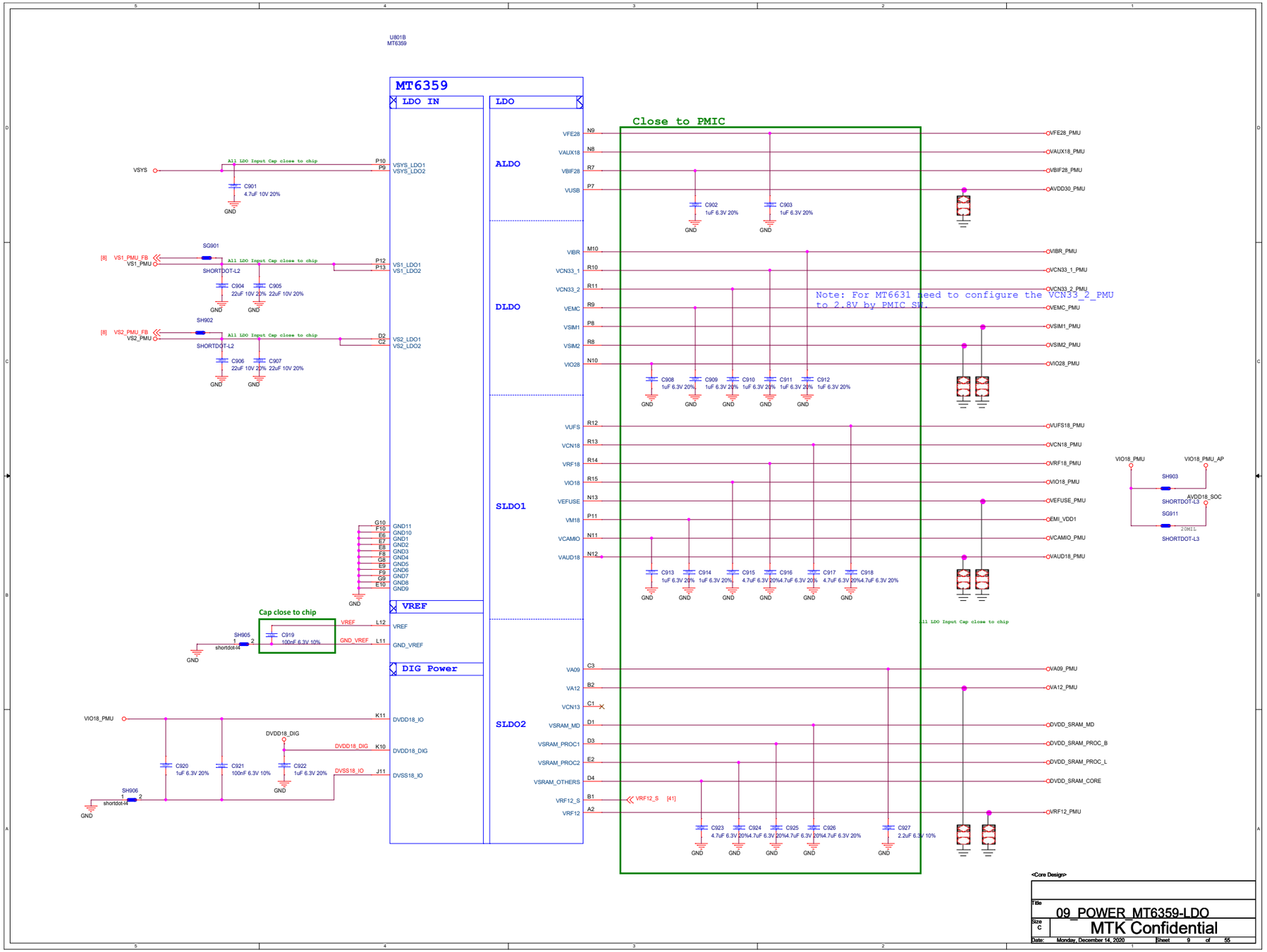

<Core Design>

Title: 09_POWER_MT6359-LDO

Size: C

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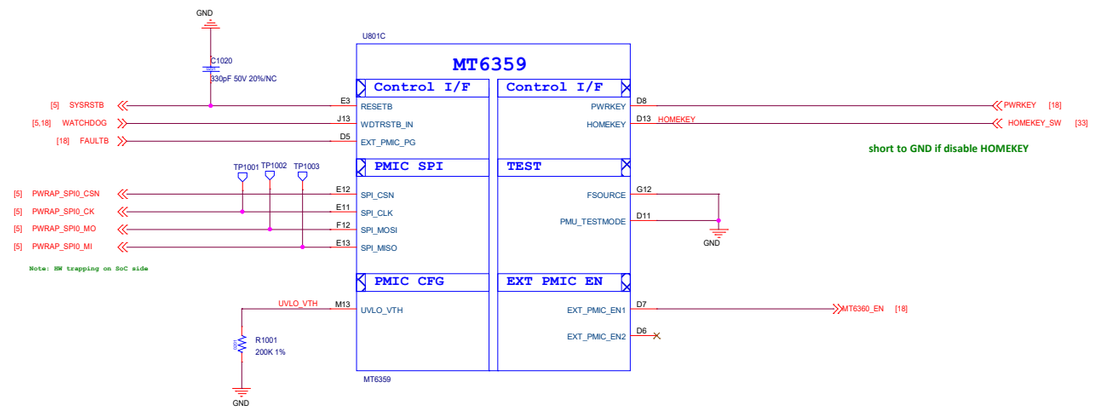

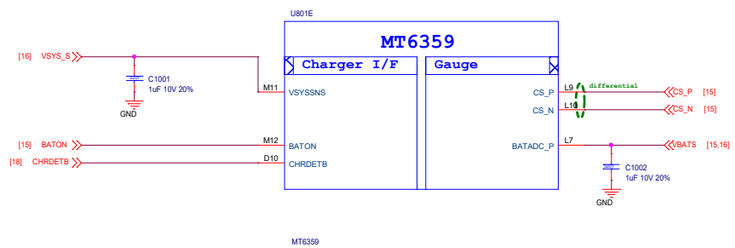

<Variant Name>

Title
10_POWER_MT6359-General

Size C

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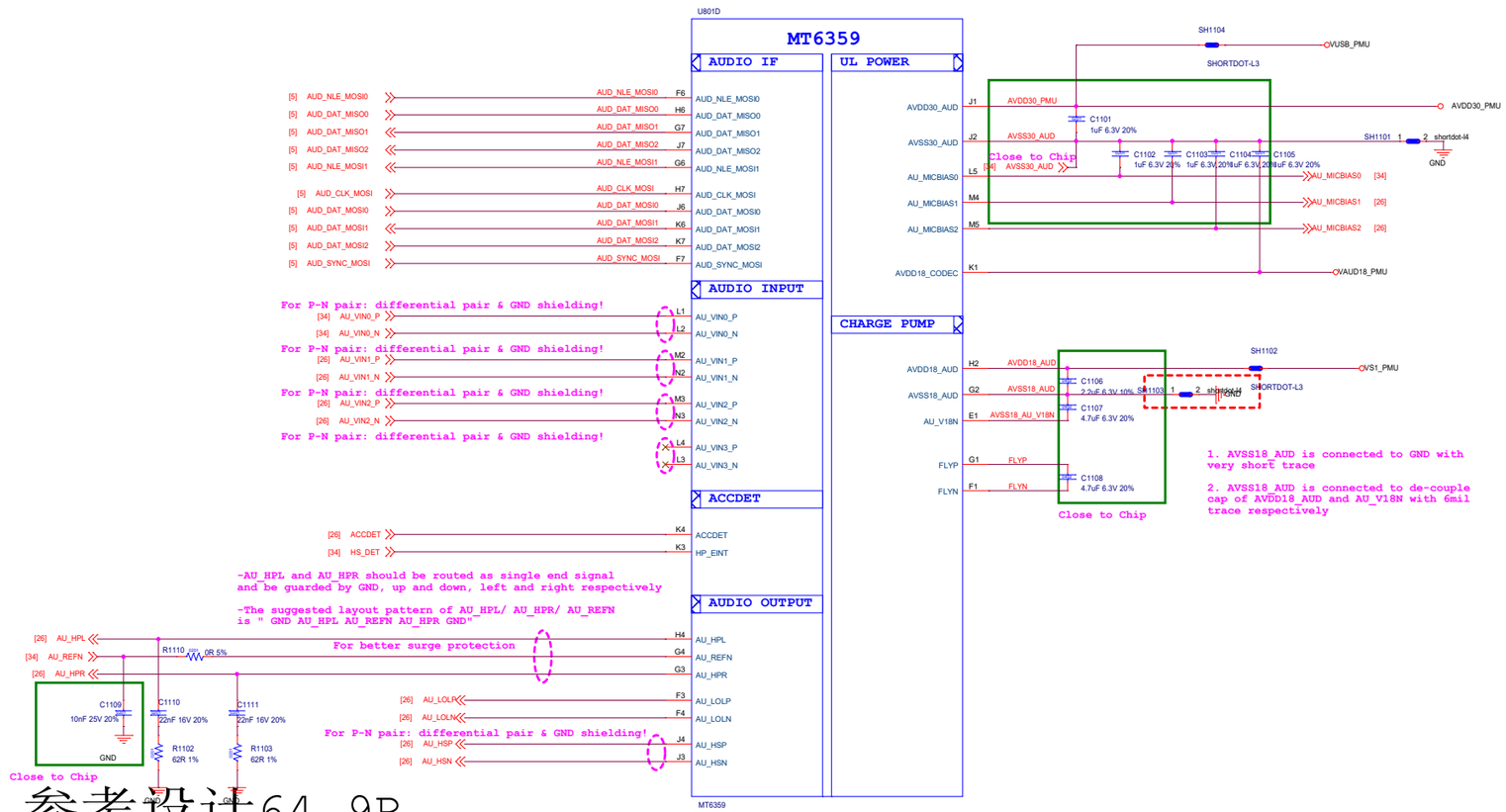
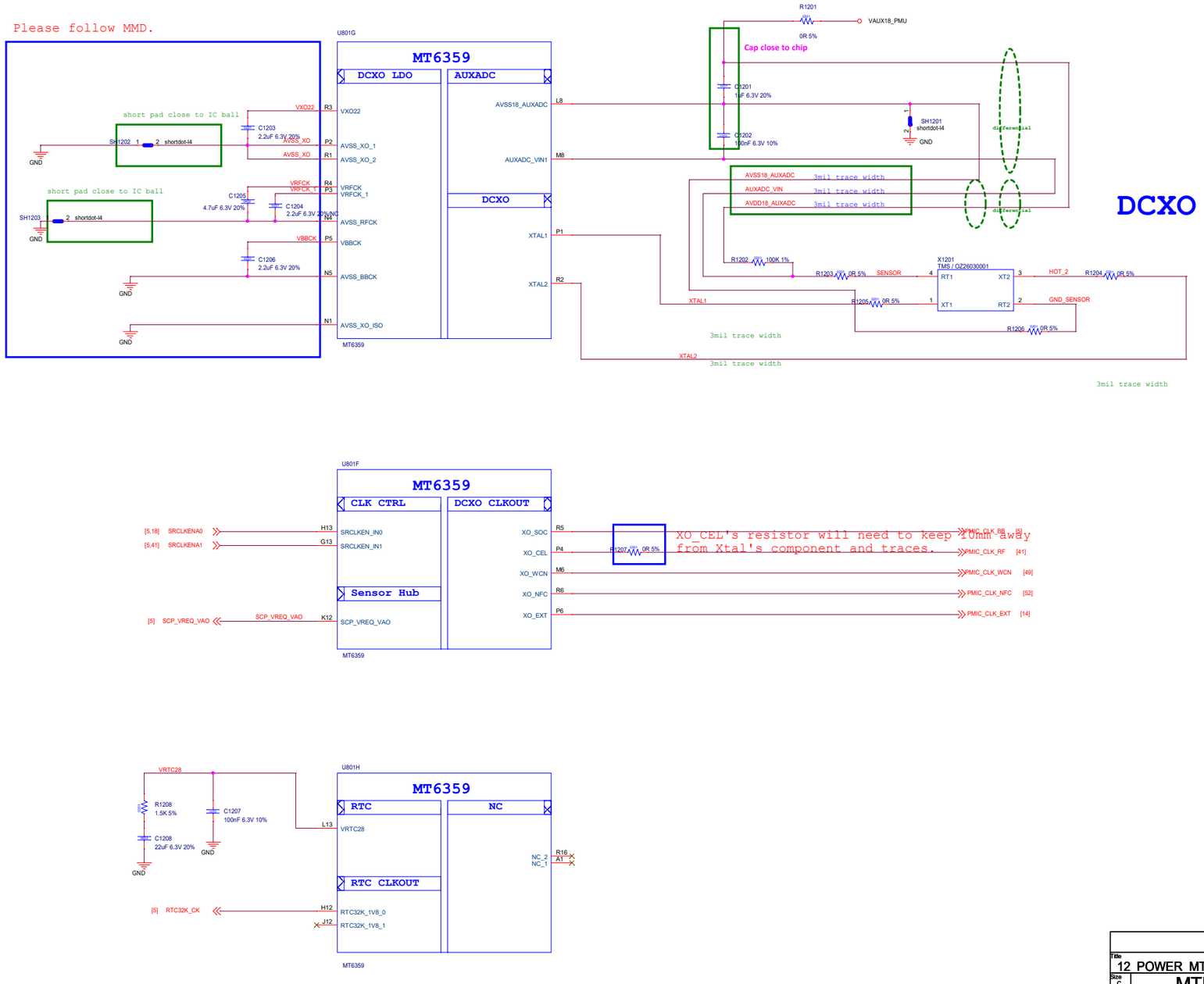
Date: Monday, December 14, 2020 Sheet 10 of 55



Title	11_POWER_MT6359_AUDIO
Size C	MTK Confidential
Date: Monday, December 14, 2020	Sheet 11 of 55



Title: 12 POWER MT6359 Clock

Size: C

MTK Confidential

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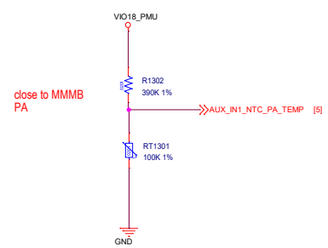
PA TEMP

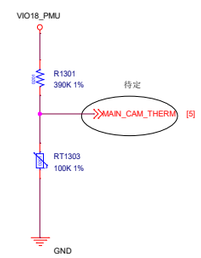
10k NTC与39k



Thermistor to sense RF PA temperature

1. RT1301 must close to LTE Band 7 PA or the hottest PA <2mm.
2. The distance is the shortest distance from package edge to edge.

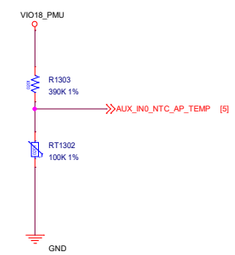
MAIN CAM



Thermistor to sense main cam temperature

1. RT1303 must close to main cam .
2. The distance is the shortest distance from package edge to edge.

AP TEMP



Thermistor to sense AP temperature

1. RT1302 must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

Title	13_NTC_Board ID
Size C	MTK Confidential
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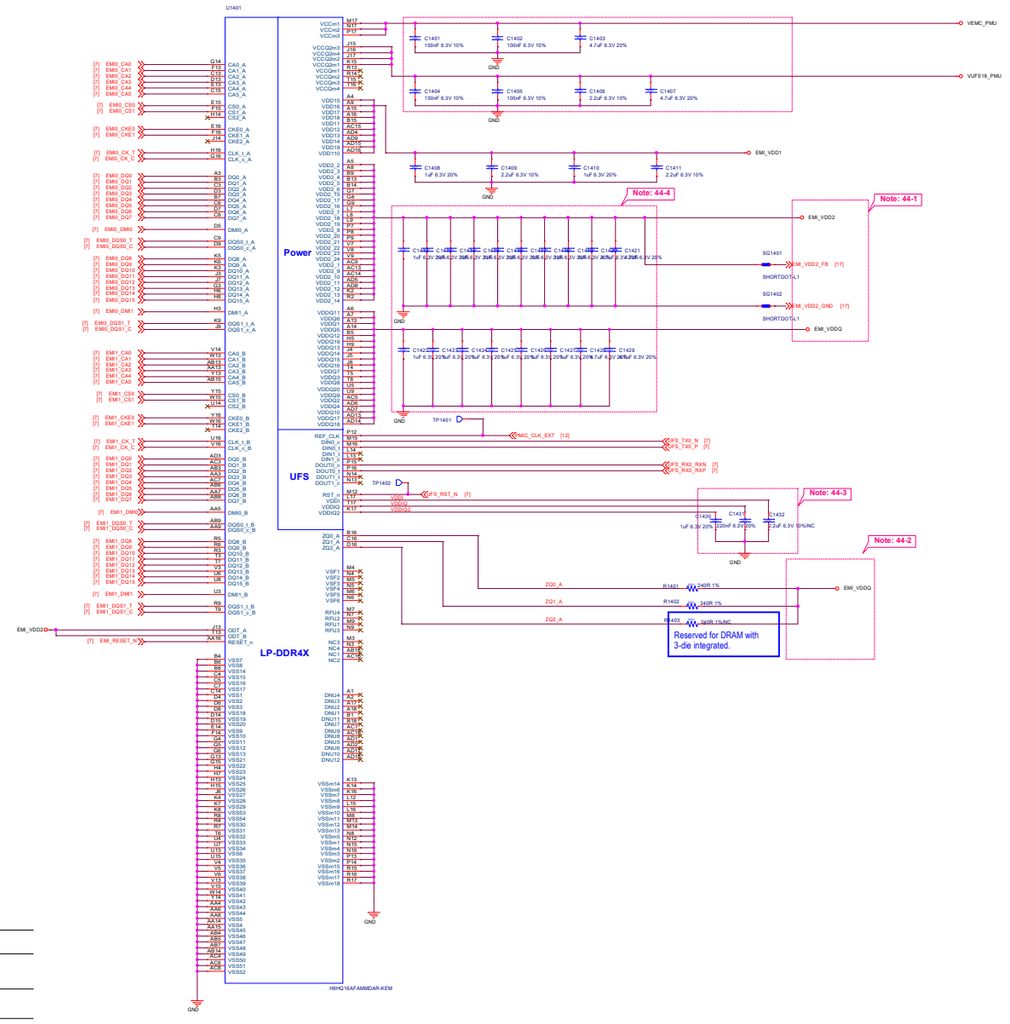

Schematic design notice of "44_Memory_UFS_LPDDR4X" page.

Note 44-1:	Please refer to power supply related page select LDO7_VOUT / BUCK2_LX output voltage properly for LPDDR4X
Note 44-2:	DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,
Note 44-3:	Please refer to uMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of UFS.
Note 44-4:	VDD2 VDDQ decoupling cap: closed to DRAM ball. For other cap for PMIC [>10uF, at PMIC page]: please also refer to MMD and layout guide for placement.

File: 14_Memory_UFS_LPDDR4X

Size: D

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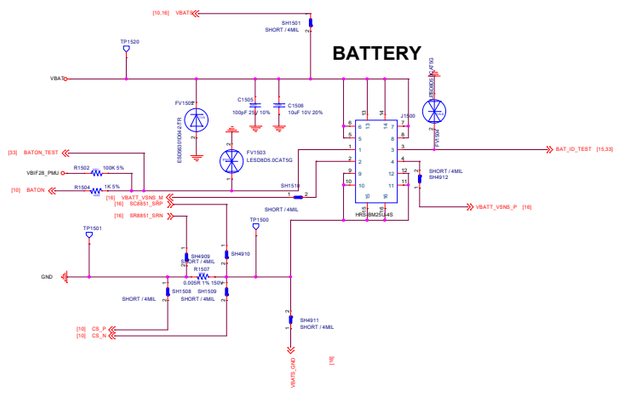

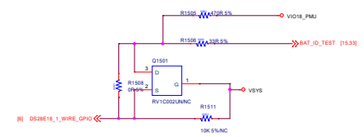

33W 加密电池

File	15_Battery Fuel guage
Size D	MTK Confidential
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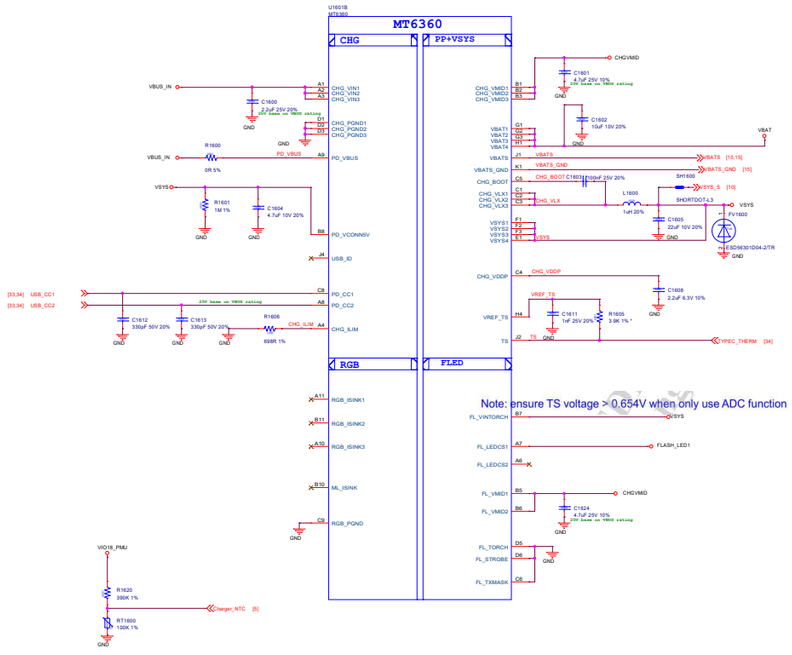

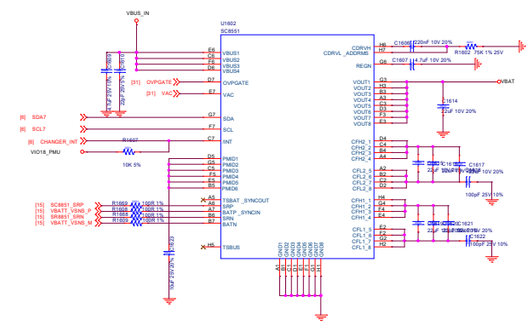

File	16_POWER_MT6360_Charger
Size D	MTK Confidential
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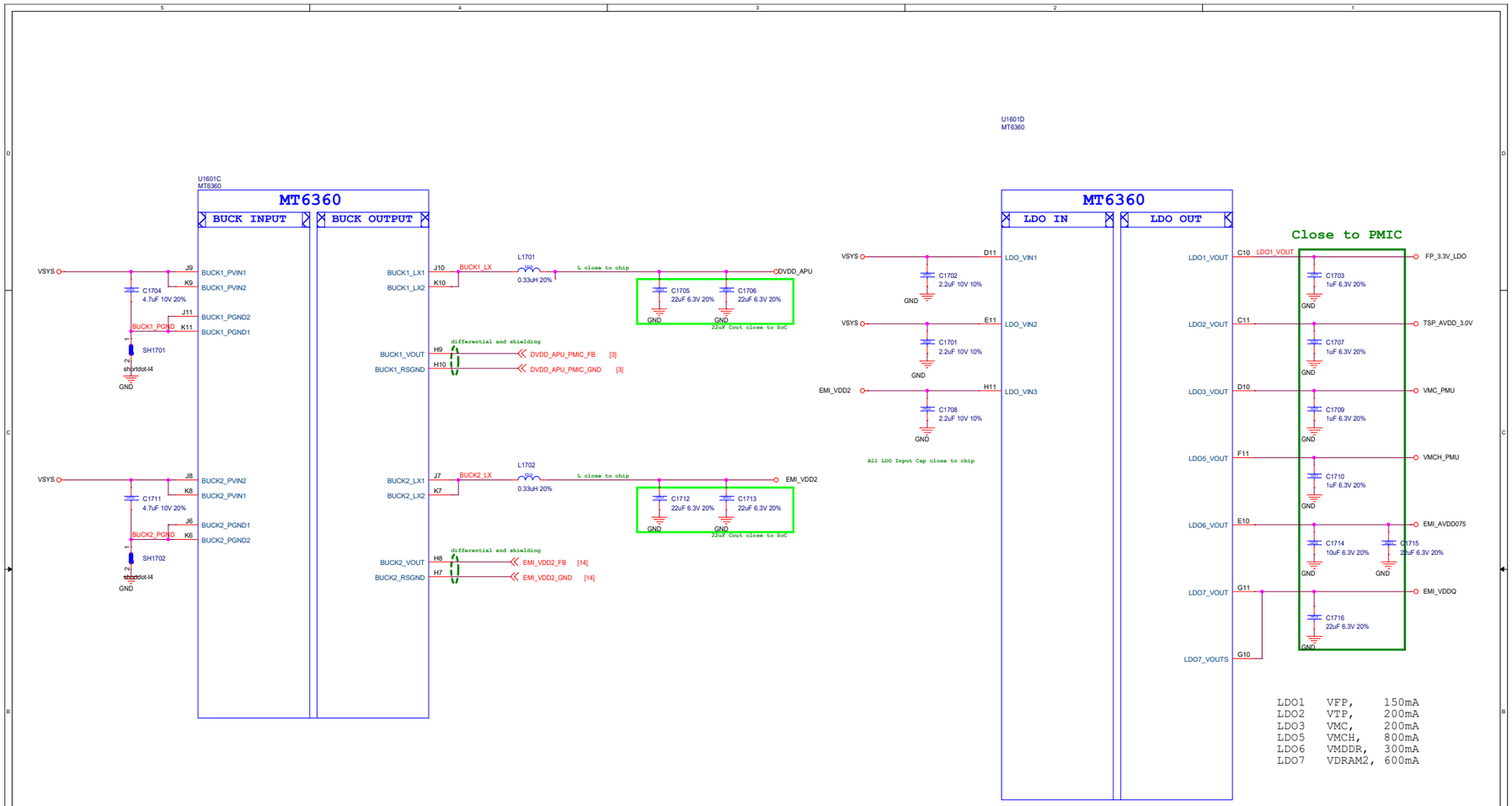

Title
17_POWER_MT6360_BUCK_LDO

Size C

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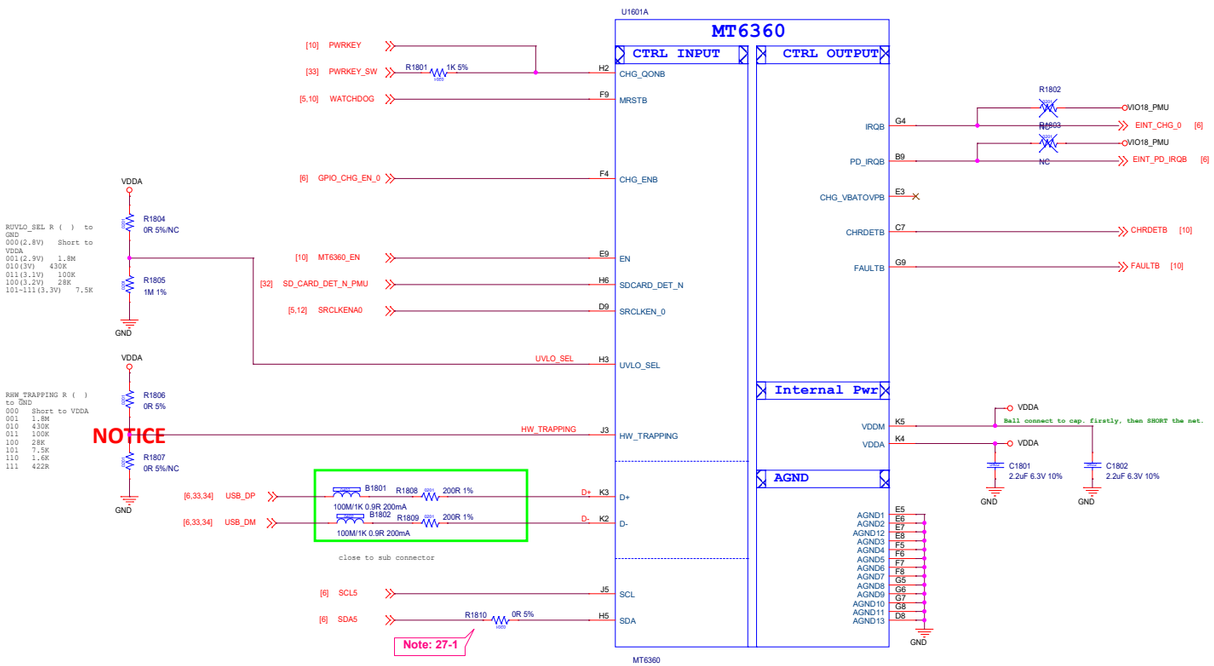

Schematic design notice of "27_POWER_MT6360_General" page:

Note 27-1: To optimize driving and PCB routing , it is recommended to reserve R for BOM fine tuning.
The R vaule and rule refer to MT6360 desing notice.

Title	18_POWER_MT6360_General
Size C	MTK Confidential
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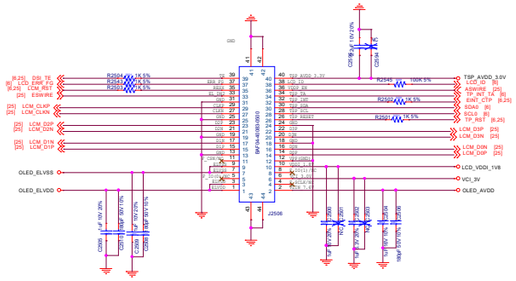

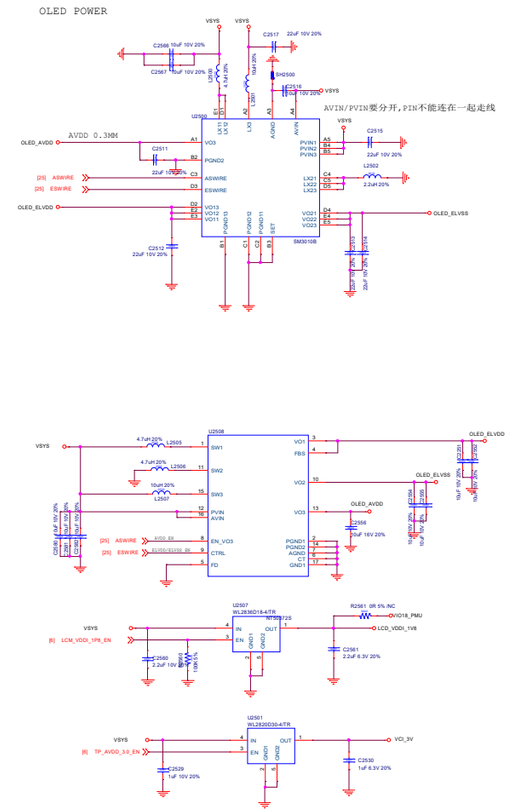

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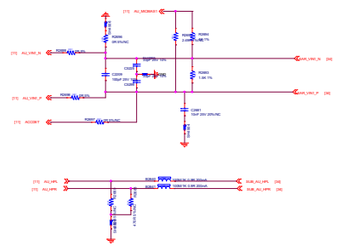
Earphone Audio



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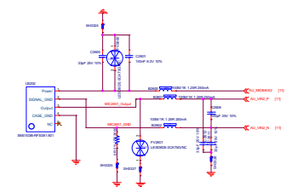

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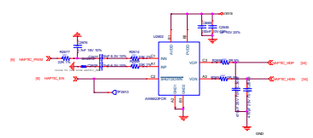

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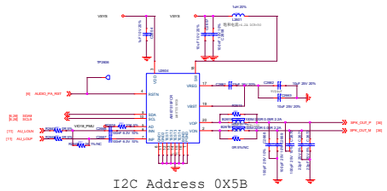

I2C Address 0X5B

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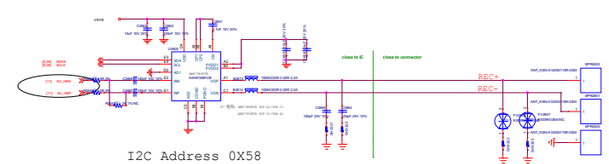
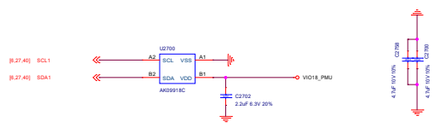
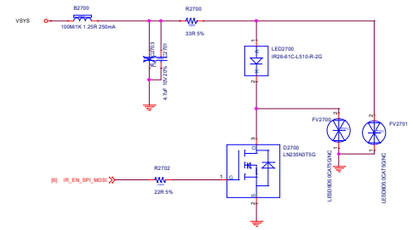


I2C Address 0X58

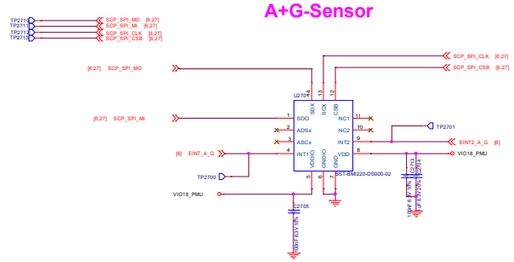
M SENSOR



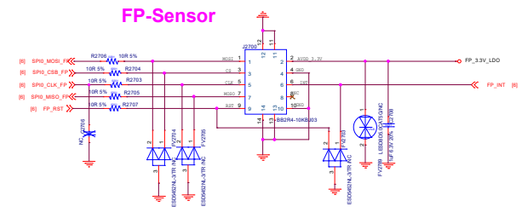
IRLED



A+G-Sensor



FP-Sensor



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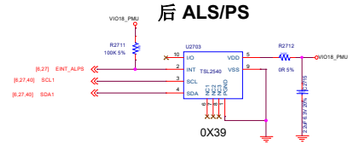

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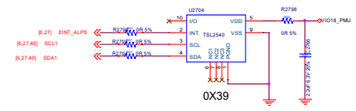

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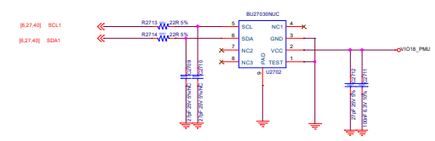

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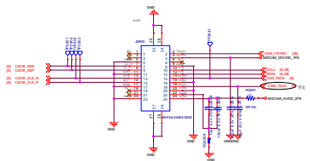
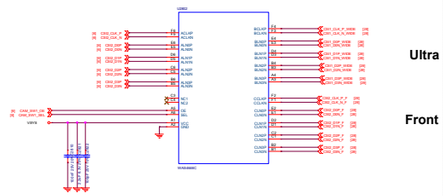
Date: Monday, December 14, 2020	Sheet 27 of 55		

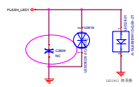
Depth Camera 2M



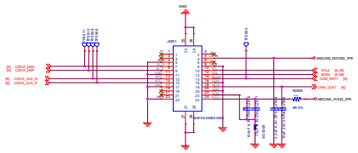
MIPI SW1



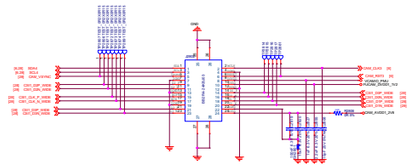
FLASH LED



Micro Camera 5M

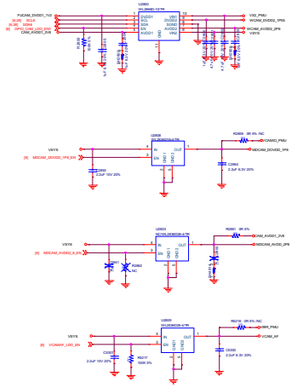


WIDE Camera 8M

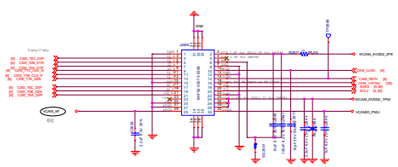


POWER LDO

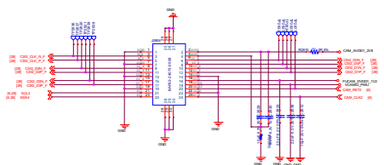
I2C Address 0X40



Main Camera 64M

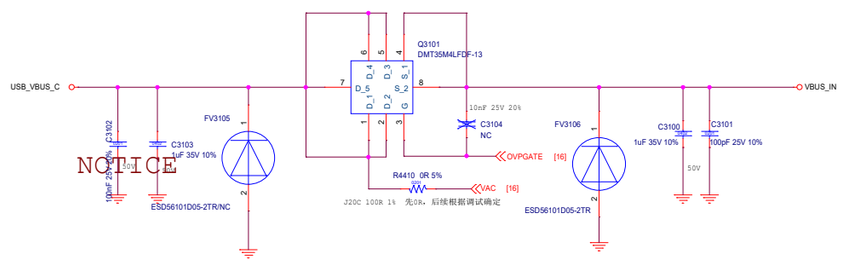


Front Camera 13M/16M



	AVDD	DVDD	IOVDD	AFVDD	I2C	MCLK	PDN	RESET
F_CAM	CAM_AVDD1_2V8	VCAM_DVDD1_1V2	VCAM0_PMU		4	MCLK2		CAM2_RST_N
B_CAM	MCAM_AVDD1_2P8	MCAM_DVDD2_1P05	VCAM0_PMU	VCAM_AF1/VBR_PMU	2	MCLK0		CAM1_RST_N
M_CAM	CAM_AVDD1_2V8		MDCAM_DOVDD_1P8		2	MCLK1		CAM1_RST_N
D_CAM	CAM_AVDD1_2V8		MDCAM_DOVDD_1P8		4	MCLK4		CAM4_RST_N
W_CAM	CAM_AVDD1_2V8	VCAM_DVDD1_1V2	VCAM0_PMU		6	MCLK3		CAM3_RST_N

OVP



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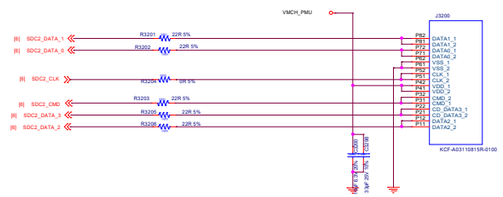
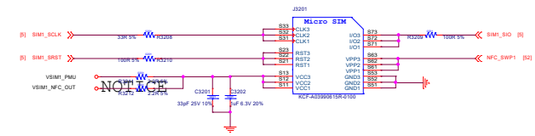
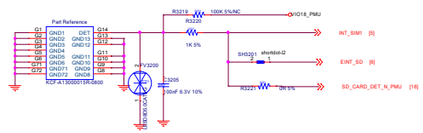
SD CARD

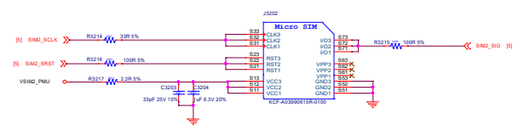


SIM1 PCB靠板边 SIM1





SIM2 PCB靠板内SIM2



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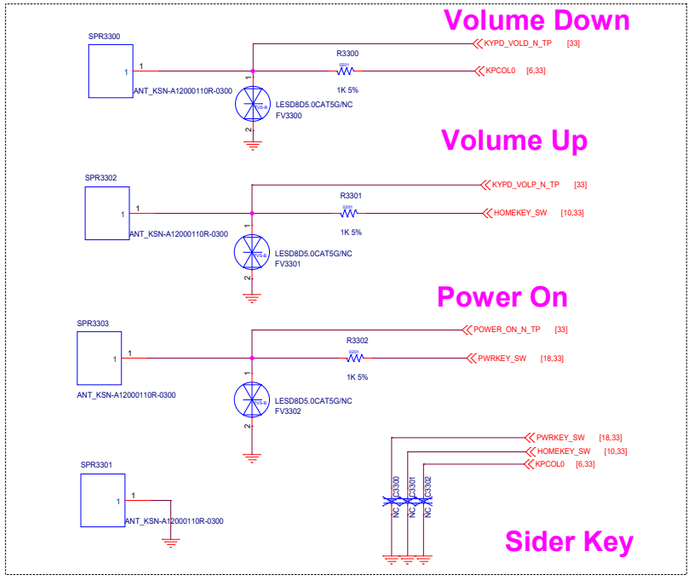

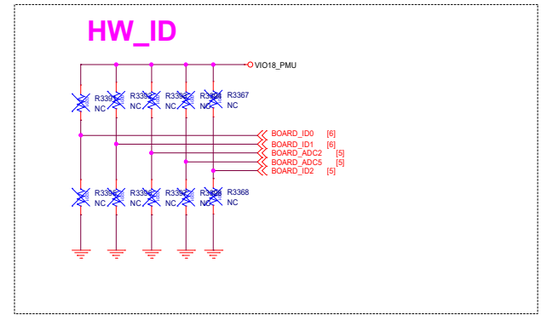

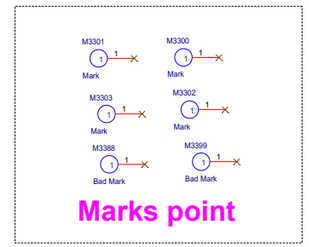

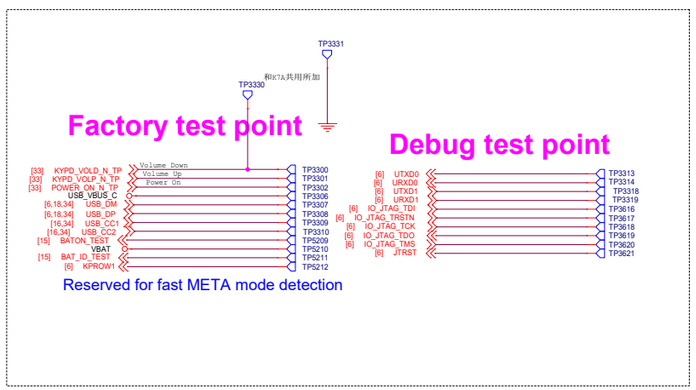

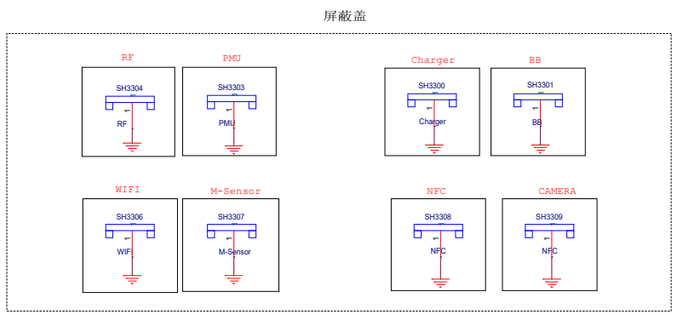

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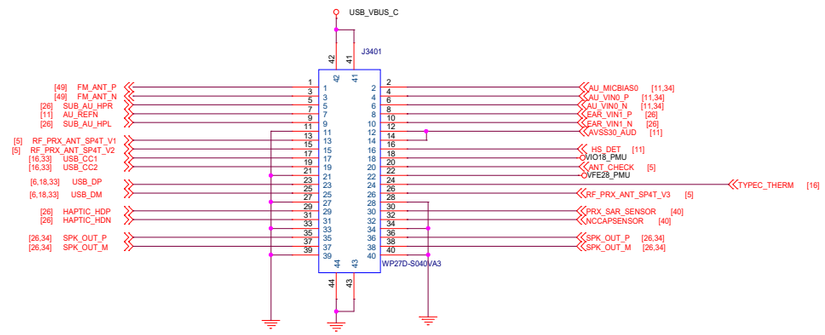
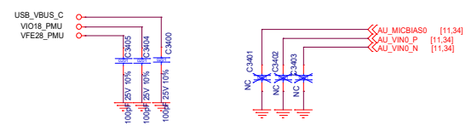


主副板连接器 1PIN位置还需要确定



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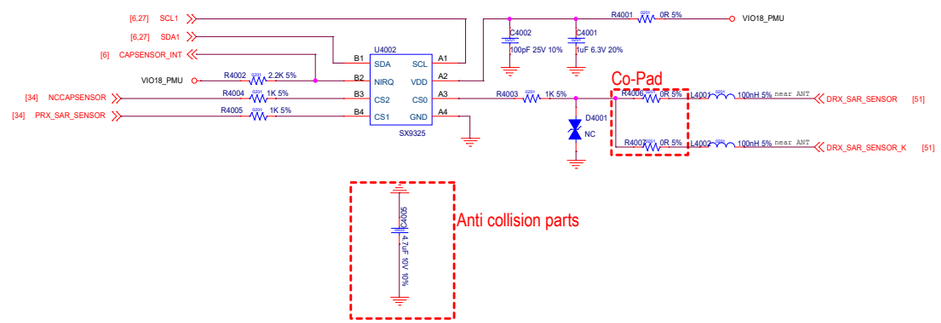
40_SAR_Sensor



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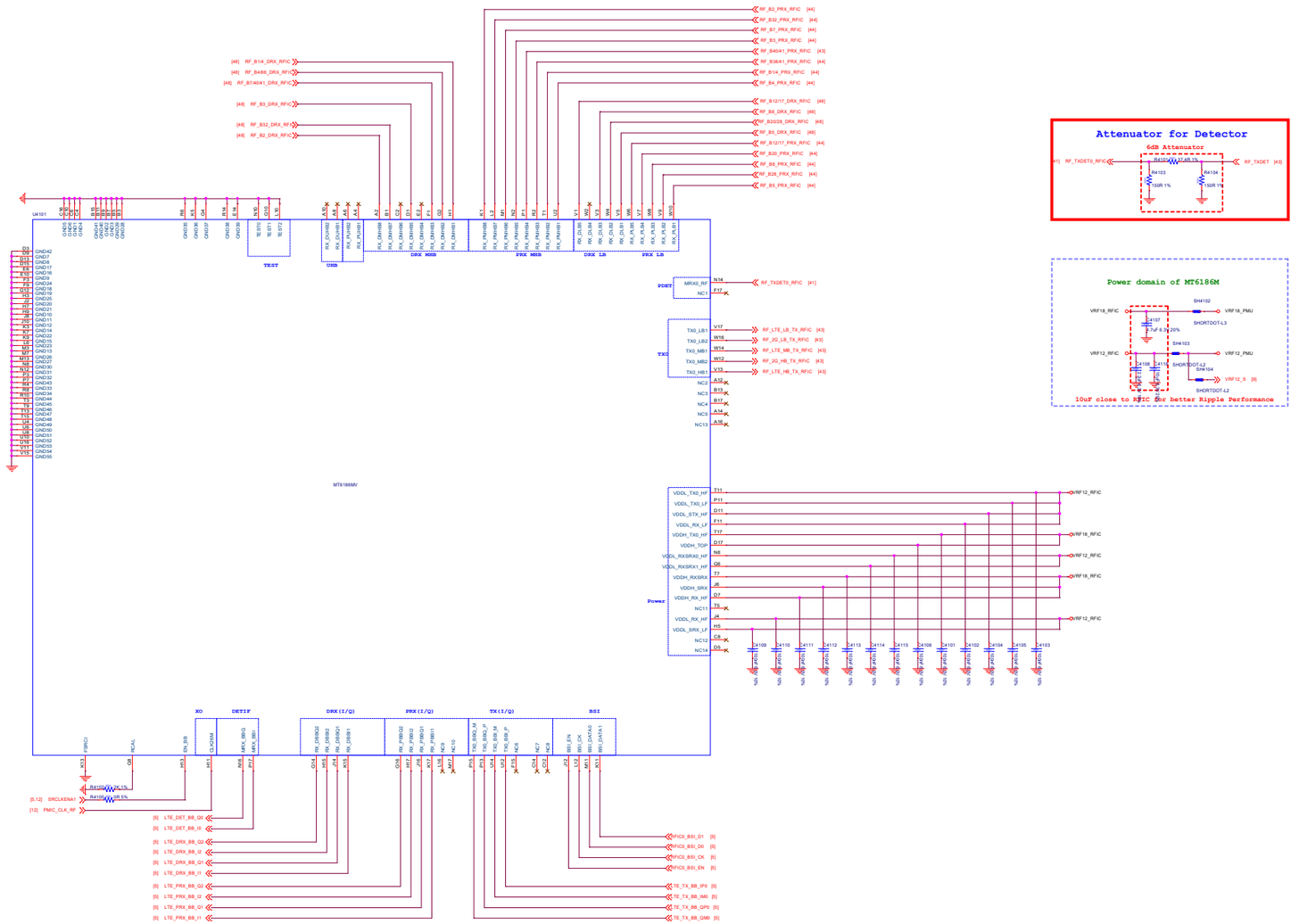
41_RF_MT6186M_Pin_Out



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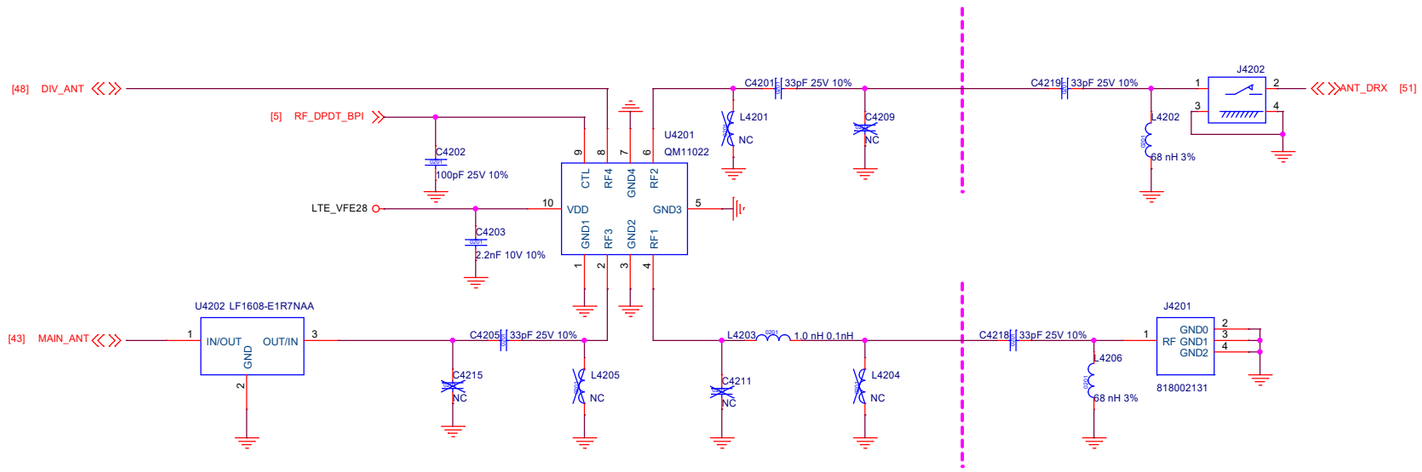
42_DPDT_Connector



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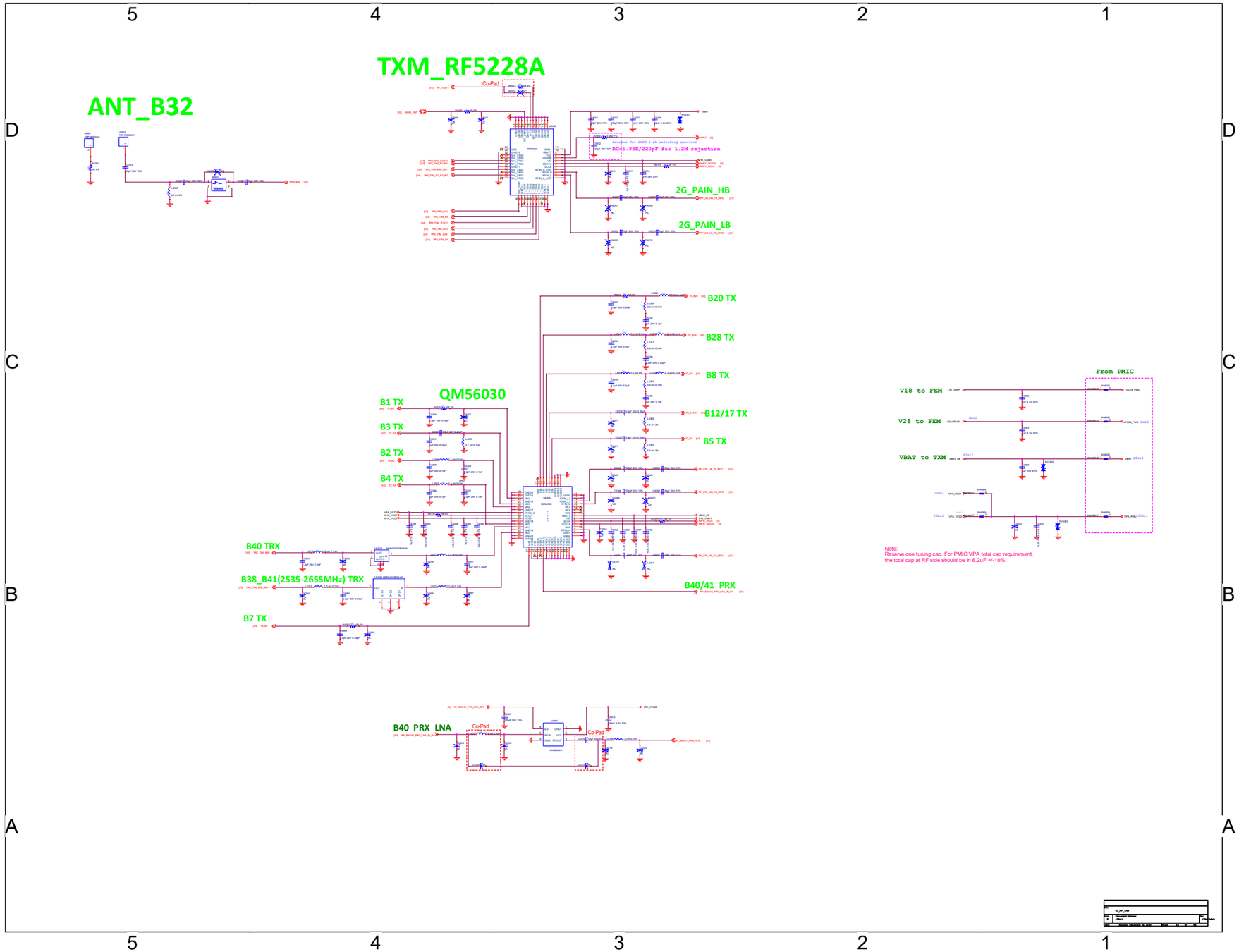
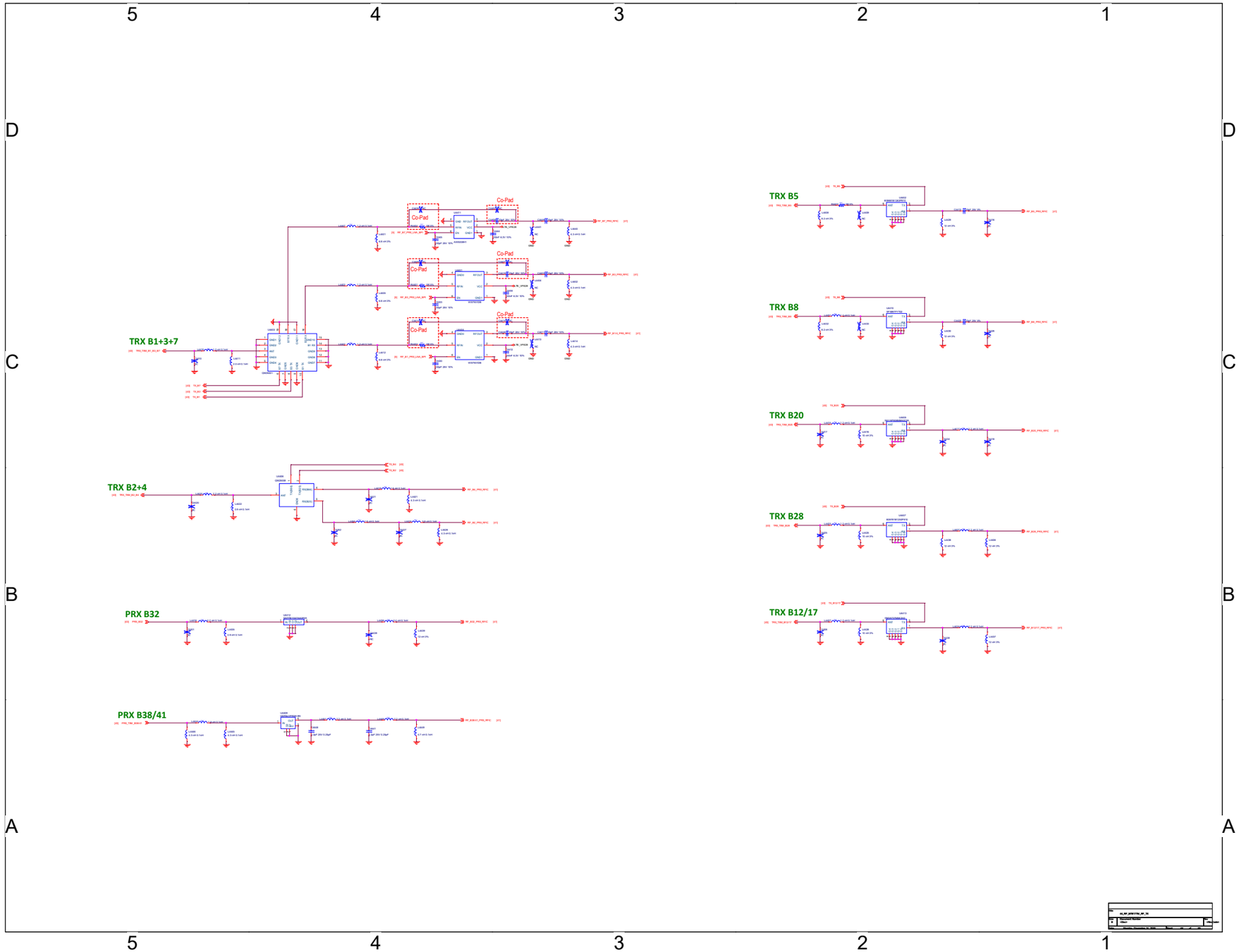
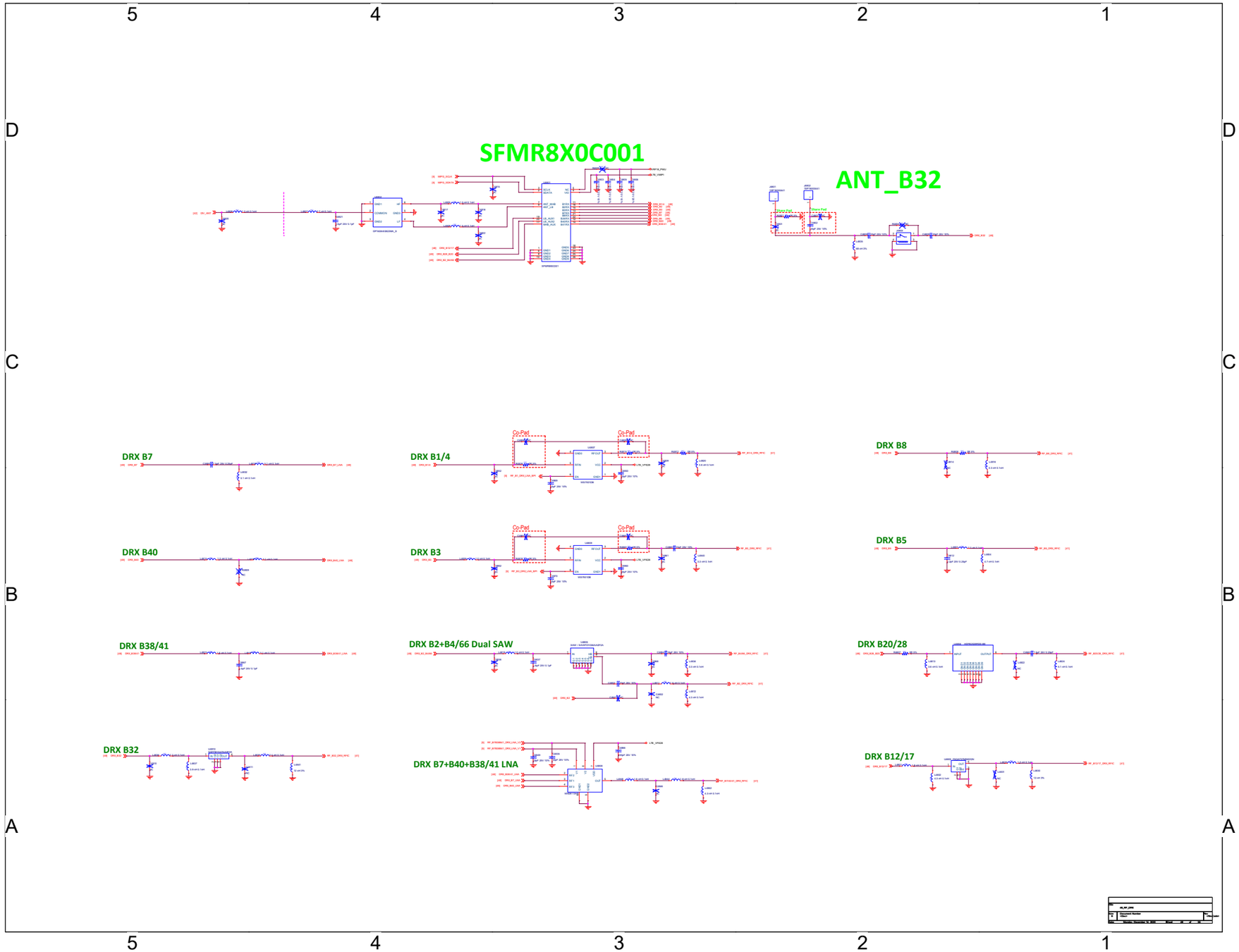
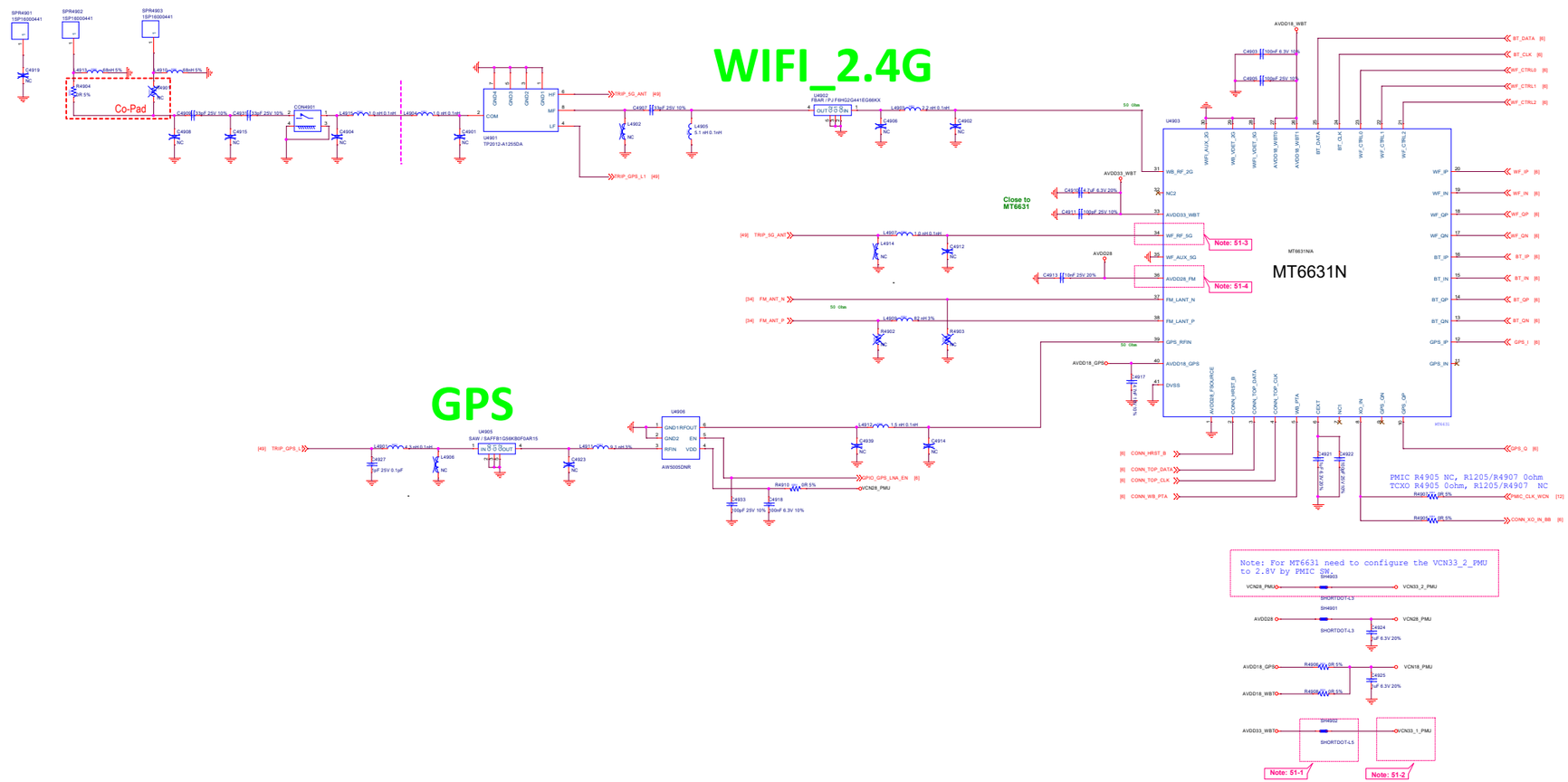

ANT_B32
TXM_RF5228A
Co-Pad
2G_PAIN_HB
2G_PAIN_LB
QM56030
B1 TX
B3 TX
B2 TX
B4 TX
B20 TX
B28 TX
B8 TX
B12/17 TX
B5 TX
B40 TRX
B38_B41(2535-2655MHz) TRX
B7 TX
B40/41 PRX
B40 PRX LNA
From PMIC
V18 to FEM
V28 to FEM
VBAT to TXM
Note:
Reserve one tuning cap. For PMIC VPA total cap requirement,
the total cap at RF side should be in 6.2uF +/-10%.

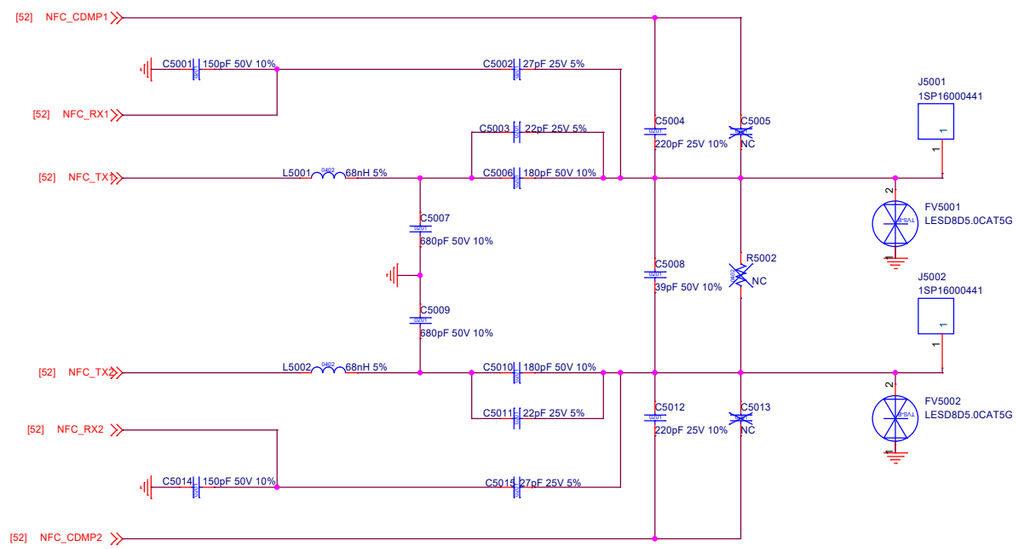

TRX B1+3+7
TRX B2+4
PRX B32
PRX B38/41
TRX B5
TRX B8
TRX B20
TRX B28
TRX B12/17
Co-Pad


SFMR8X0C001
ANT_B32
DRX B7
DRX B1/4
DRX B8
DRX B40
DRX B3
DRX B5
DRX B38/41
DRX B2+B4/66 Dual SAW
DRX B20/28
DRX B32
DRX B7+B40+B38/41 LNA
DRX B12/17
Co-Pad
Co-Pad



Note 51-1:	For R3712 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6765 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support

50_ANT_NFC



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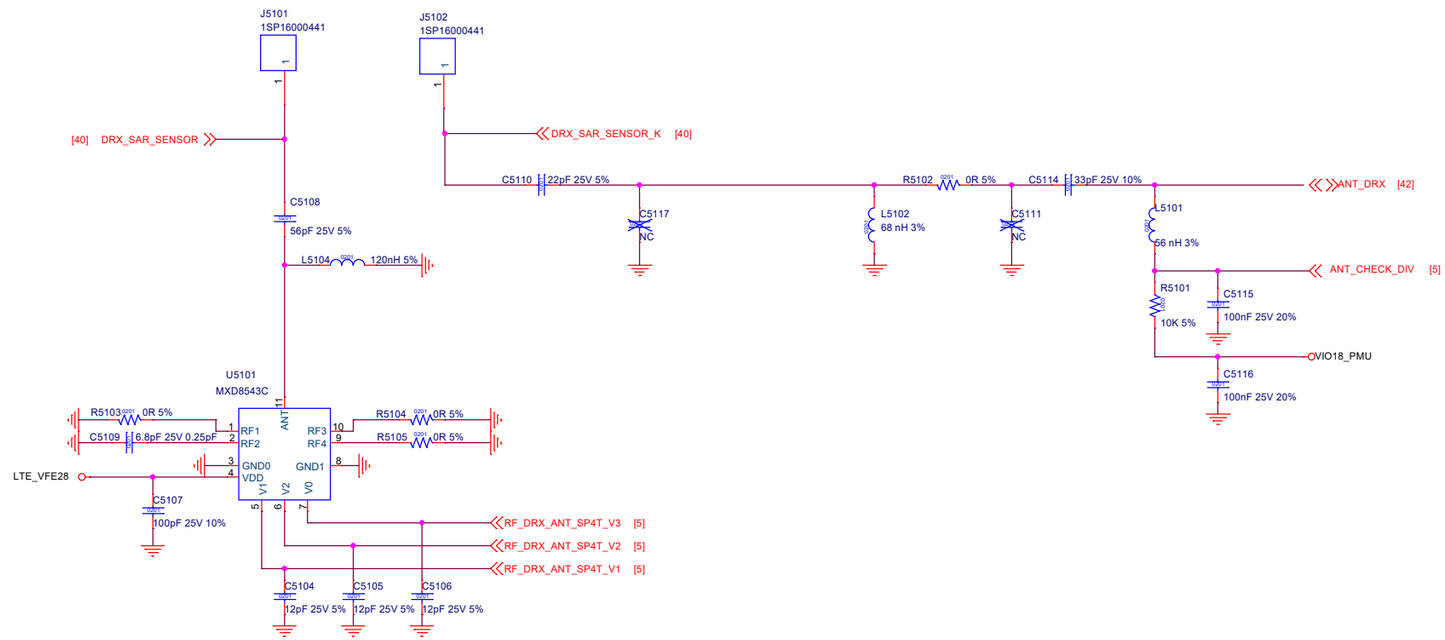
51_ANT_DIV



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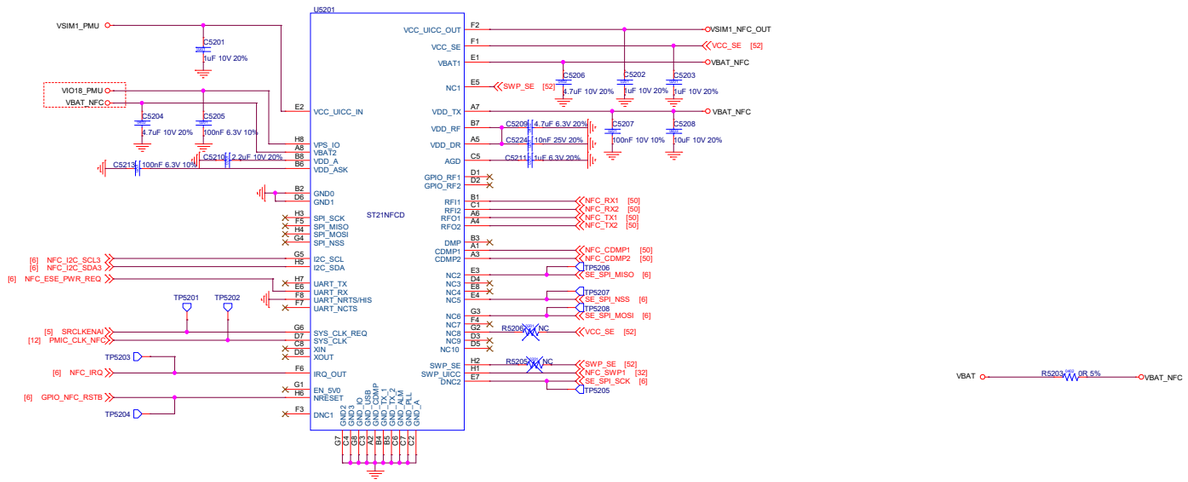
52_NFC



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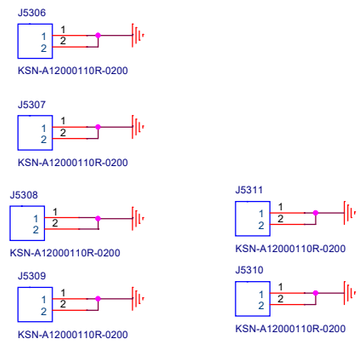
53_ANT_TOP_GND



主板接地弹片

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